CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-7 (canceled).

Claim 8 (currently amended). A memory configuration, comprising:

a memory matrix including a plurality of memory cells connected to one another, said memory cells including ferroelectric transistors such that at least some of said memory cells each include at least a respective one of said ferroelectric transistors;

a read/store control apparatus connected to said memory cells for controlling one of reading a state from one of said ferroelectric transistors and storing a state to said one of said ferroelectric transistors; and

said read/store control apparatus being configured such that the state is one of read from said one of said ferroelectric transistors and stored in said one of said ferroelectric transistors, and such that a threshold voltage of at least a further one of said ferroelectric transistors in said memory

matrix is increased by applying a drain-substrate voltage.

Claim 9 (original). The memory configuration according to claim 8, wherein:

said one of said ferroelectric transistors has a gate electrode; and

said read/store control apparatus is configured such that a read voltage is applied to said gate electrode for reading the state from said one of said ferroelectric transistors.

Claim 10 (original). The memory configuration according to claim 8, wherein:

said one of said ferroelectric transistors has a gate electrode; and

said read/store control apparatus is configured such that a store voltage is applied to said gate electrode for storing the state in said one of said ferroelectric transistors.

Claim 11 (original). The memory configuration according to claim 8, wherein at least one of said memory cells in said memory matrix includes at least two transistors.

Claim 12 (currently amended). The memory configuration according to claim 8, wherein said read/store control apparatus is configured such that the threshold voltage of said further one of said ferroelectric transistors in said memory matrix is increased by applying ~~a~~ the drain-substrate voltage to said further one of said ferroelectric transistors in said memory matrix.

Claim 13 (original). The memory configuration according to claim 12, wherein said read/store control apparatus is configured such that the drain-substrate voltage is substantially +3.3 volts.

Claim 14 (original). The memory configuration according to claim 12, wherein said read/store control apparatus is configured such that the drain-substrate voltage is substantially -3.3 volts.

Claim 15 (new). The memory configuration according to claim 8, wherein the applied drain-substrate voltage forms a plateau in a hysteresis loop of said further one of said ferroelectric transistors to define a ferroelectric polarization profile.